

ABSTRACT OF THE DISCLOSURE

A PDP address data processor, a method thereof, and a recording medium for storing a program used to perform the method. The address data processor generates subfield data corresponding to RGB input video data, divides them into two sets of subfield data, and stores them in a frame memory using rising and falling edges of a reference clock signal of a frame memory. The address data processor reads and arranges the stored subfield data using the rising and falling edges to generate address data for representing gray on the PDP. The address data processor uses an RGB mixing algorithm for selecting two different video data from among the RGB input video data to select video data, and generates the subfield data corresponding to the selected video data.

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